IN THE CLAIMS

1. (Currently amended) A data processing apparatus, the apparatus comprising:

an input port for receiving a communication signal that contains temporally successive bits;

an output port for outputting a data word formed from respective ones of the temporally successive bits;

a programmable processor circuit coupled to the input port, the processor executing a plurality of series of programmed instructions in support of said receiving ~~and~~ or said outputting, each at a time of reception of a respective one of the temporally successive bits, the processor circuit suspending operation each time after executing a respective one of the series of instructions;

a synchronization circuit coupled to the processor circuit to trigger execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.

2. (Currently amended) A data processing apparatus according to claim 1, wherein the programmable processor is programmed to compute cumulative information, corresponding to a function of a combination of the bits from which the data word is formed, each series of instructions being programmed to add a contribution to the cumulative information of the respective one of the temporally successive bits at the time of reception of which the series is executed.

3. (Previously presented) A data processing apparatus according to claim 2, wherein said cumulative information comprises one or more parity bits.

4. (Currently amended) A data processing circuit according to claim 1, wherein the processor circuit is constructed sequence instruction execution using handshake signals, execution of each of the instructions of the series being triggered by a respective request signal, execution of each instruction of the series, except for a last instruction in each series, generating the request signal for a next one of the instructions in the series, the synchronization circuit being coupled to apply the request signals for the initial one of the instructions in the series.

5. (Previously presented) A data processing apparatus according to claim 1, wherein the synchronization circuit contains an adaptable timer circuit, arranged to adapt a frequency of triggering the execution of the series of instructions under control of a timing of transitions in the communication signal.

6. (Currently amended) A data processing apparatus according to claim 5, wherein the adaptable timer circuit is arranged to measure a duration of a synchronization interval in the communication signal preceding ~~the~~ bits that contribute to the data word, and to set the frequency that will be used to trigger execution of the series of instructions dependent on the measured duration.

7. (Currently amended) A data processing apparatus according to claim 6, wherein the

timer circuit is arranged to detect ~~the~~ presence or absence of a validation part in the communication signal prior to ~~the~~ bits that contribute to the data word, the timer circuit generating ~~the~~ execution trigger signals only upon detection of the presence of the validation part.

8. (Previously presented) A data processing apparatus according to claim 1, wherein the processor circuit is designed to execute only instructions with one bit operand data.

9. (Currently amended) A method of processing data, the method comprising:

receiving a communication signal that contains temporally successive bits;

outputting a data word derived from a plurality of the successive bits;

executing a plurality of series of programmed instructions in support of receiving and/or outputting, each at a time of reception of a respective one of the temporally successive bits, suspending execution of the series of instructions each time after executing a respective one of the series of instructions;

triggering execution of respective ones of the series of instructions, each time at the time of reception of the respective one of the temporally successive bits, and, except for a last one of the series of instructions, prior to reception of one or more later bits that contribute to the data word.